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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,697	07/15/2003	Karen L. Noel	200312434-1	7142

22879 7590 02/09/2007

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EXAMINER	
PATEL, KAUSHIKKUMAR M	
ART UNIT	PAPER NUMBER
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	02/09/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/619,697
Filing Date: July 15, 2003
Appellant(s): NOEL ET AL.

Mark E. Scott
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 06, 2006 appealing from the Office action mailed May 04, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

Claims 1-2 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Harvey et al. (US 6,233,668).

Claims 3-19 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Harvey et al. (US 6,233,668) and further in view of de Backer et al. (US 6,266,745).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,233,668	Harvey et al.	05-2001
6,266,745	de Backer et al.	07-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harvey et al. (US 6,233,668 B1) (Harvey herein after).

Regarding claim 1, Harvey teaches a method of running multiprocessor system (fig. 2) with replicated data and operating systems on all the processing nodes (column 3, lines 37-40) using virtual memory address (VMA) (column 1, lines 44-60) and runs a instances of programs with their respective page tables (fig. 1). Harvey implicitly failed to teach claim 1, but it obvious to one having ordinary skill in the art at the time of the invention that, multiprocessor system (fig. 2) running replicated versions of data and operating systems (column 3, lines 37-40) can execute a first instance of a program

(operating system) on a first processor (fig. 2, item 48) and second instance of the program on second processor (fig. 2, item 50) and maintain respective page tables in respective memories. Also since, system uses virtual memory addressing it also obvious that during execution of the instance of the program refers to memory address using page tables and pointers to refer to same physical memory address using VMA (column 2, lines 23-33).

Regarding claim 2, Harvey teaches that data and operating system program is replicated in individual memories of the processor to reduce the cost of the non-uniform access times (column 3, lines 37-40), thus Harvey teaches a functional unit with replicated versions of the same program running respective instances of the programs.

Claims 3-7 and 8-19 are rejected under **35 U.S.C. 103(a)** as being unpatentable over Harvey et al. (US 6,233,688 B1) as applied to claims 1 and 2 above, and further in view of de Backer et al. (US 6,266,745 B1) (Backer herein after).

Harvey teaches a method of multiprocessor system running replicated versions of data and operating system as applied to claims 1 and 2 above, but fails to teach use of performance counters. Backer teaches a method of multiprocessor system running same operating systems on each node (see abstract). Backer also teaches a counter (fig. 1, items 26, 28 and 30), which keeps track of the shared memory accesses by each threads (column 3, lines 45-65). It would have been obvious to one having ordinary skill in the art at the time of the invention would have used the teachings of Backer to keep

track of memory accesses using counters in the system of Harvey to determine utilization of the node by use of counters (Backer, column 2, lines 30-40) to allocate (replicate) frequently used memory in the respective nodes and thus improving system performance.

As per claim 4, Backer teaches an individual counter, which keeps track of memory accesses for individual node (fig. 1, column 3, lines 59-67 and column 4, lines 1-7). Backer fails to teach combining the counter value. It would have been obvious to one having ordinary skill in the art at the time of the invention would combined the all counter values to get total utilization of the whole system.

As per claims 5-7, Backer fails to teach keeping counter values for page allocations, disk accesses and look-aside list. It is well known that page table allocations; disk accesses and look-aside lists are parts of the memory accesses in the virtual memory addresses. It would have been obvious to one having ordinary skill in the art at the time of the invention would have used the counters for page allocations, disk accesses (kind of memory access) and look-aside lists to get precise utilization and to better allocate resources to individual nodes.

Claims 8-19 are also rejected under same rationale as applied to claims 1-7 above. The read/write variable as mentioned in the claims 8-10 are considered as counters from the description of the present application specification (page 5, paragraph [0015]).

(10) Response to Argument

Applicant essentially provides one argument.

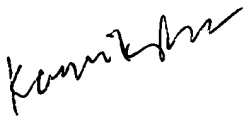
(1) Harvey discusses the duplication of "shared code and read-only data" and Harvey does not appear to address or be operational with duplication of "writable data", as highlighted throughout the appeal brief (pages 11-13). In response to applicant's argument, Examiner asserts that, Harvey provides background on non-uniform access times for accessing memory located at different places, e.g. local and remote memories and Harvey further asserts that cost of accessing local memory is relatively low with respect to remote memory (see Harvey, col. 2, line 51 – col. 3, line 8). To overcome this disadvantage Harvey suggests replicating process's code and data in different locales (Harvey, col. 3, lines 30-40). Harvey further imposes a limitation saying, "Replicating all such code and data is clearly impractical" because "such general policy (of replicating data and code) would impose an intolerable synchronization overhead for read/write data" and such overhead would compromise the intended performance (Harvey, col. 3, lines 40-46). Harvey further teaches that, "Still significant benefits can result if a replication policy is implemented selectively" by replicating operating system's code and read-only data (Harvey, col. 3, lines 46-53). The purpose of replicating operating system code and read-only data is to overcome the performance degradation due to maintaining synchronization/coherency of read/write data. It is clear from forgoing statements that read/write data (writable data of the applicant) carries significant overhead of maintaining synchronization/coherency, which can offset the advantage of reducing memory access costs, and as per applicant's specification, the writable data

do not require such synchronization/coherency (see, present application specification, page 5, par. [0015], lines 7-8, "coherence protocol need not extend to maintain coherence among the various RADS with respect to those duplicated writable memory areas"). As explained above, Harvey teaches replicating read-only (because they do not require any coherence protocol) data and accordingly one having ordinary skill in the art at the time of the invention would be motivated to replicate any data (including writable data as claimed by the applicant) that do not require any synchronization/coherency overhead to improve system performance by reducing non-uniform memory access times. Also during the reply to first office action, applicant did not consider this limitation (writable data) as critical because during the response applicant was arguing about Harvey not teaching "VMA in each functional unit is same" as highlighted in remarks section on applicant's reply filed on March 31, 2006 in response to first office action mailed February 02, 2006. The remaining limitations "wherein the program refers to a virtual memory address (VMA) in a page table to obtain a pointer to a memory location to write data" is mere a process of converting virtual address to a physical address and since Harvey teaches use of virtual memory addressing (Harvey, col. 1, line 33 – col. 2, line 7), the recited limitation is inherent in Harvey's system. Harvey also teaches VMA referred by first and second instance is same (Harvey, col. 2, lines 23-34).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Kaushik Patel.



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